CLAIMS

1. A memory device having equalized bitline capacitance; comprising:

a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline;

a core cell having a bitline and a complementary bitline;

a flipped core cell that has a flipped bitline and a flipped complementary bitline, the multiple pairs of the global bitline and the global complementary bitline have a plurality of core cells that are defined by alternating ones of the core cell and the flipped core.

2. A memory device having equalized bitline capacitance as recited in claim 1, wherein the bitline of the core cell is coupled with the flipped complementary bitline of the flipped core cell, and the complementary bitline of the core cell is coupled to the flipped bitline of the flipped core cell.

3. A memory device having equalized bitline capacitance as recited in claim 2, wherein successive pairs of the core cell and the flipped core cell are aligned along each of the multiple pairs of the global bitline and the global complementary bitline.

4. A memory device having equalized bitline capacitance as recited in claim 3, wherein the core cell and the flipped core cell have an identical pair of cross-coupled inverters.

5. A memory device having equalized bitline capacitance as recited in claim 4, wherein each of the identical pair of cross-coupled inverters includes two P-type transistors and two N-type transistors.

6. A memory device having equalized bitline capacitance as recited in claim 4, wherein each of the core cell and the flipped core cell have a pair of passgate transistors that are coupled to a respective one of the plurality of words.

7. A memory device having equalized bitline capacitance as recited in claim 1, wherein the memory device laid-out on multiple layers of a semiconductor device.

8. A memory device having equalized bitline capacitance as recited in claim 7, wherein the core cell and the flipped core cell have cross-coupled inverters that include four transistors, the four transistors have gates that are laid out in polysilicon and cross-coupling connections that are at least partially connected through a multi-layer interconnect structure.

9. A memory device having equalized bitline capacitance as recited in claim 8, wherein when the cross-coupling connections are at least partially connected through a multi-layer interconnect structure, the core cell and the flipped core cell layout sizes are substantially reduced.

10. A memory device having equalized bitline capacitance as recited in claim 1, further comprising:

a memory generator for designing the memory device.

11. A memory device; comprising:

a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline;

a core cell having a bitline and a complementary bitline;

a flipped core cell that has a flipped bitline and a flipped complementary bitline; and

a plurality of the core cell in a column and a plurality of the flipped core cell are arranged in the column, such that the plurality of the core cell equals the plurality of the flipped core cell.